IN THE CLAIMS

1. (currently amended): An intermediary of a semiconductor device, comprising:

a semiconductor substrate having a surface formed with a first recessed region;

a first dielectric material formed in the first recessed region;

a second recessed region formed within the first dielectric material, wherein the second recessed region has walls, a lower surface, and a first opening in proximity to the surface; and

a polycrystalline semiconductor layer formed overlying the first dielectric material and having a second opening at least partially overlying ~~over~~ the first opening, wherein the polycrystalline semiconductor layer and the second recessed region are configured to form a region of reduced substrate capacitance. ~~is configured to at least partially convert to an oxide layer that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is subsequently exposed to an oxidizing environment to form the oxide layer.~~

Claims 2-4 (cancelled).

5. (currently amended): The intermediary ~~semiconductor device~~ of claim 1, wherein the polycrystalline semiconductor layer comprises polysilicon.

6. (currently amended): The intermediary ~~semiconductor device~~ of claim 1, wherein the first dielectric material includes deposited silicon dioxide.

7. (currently amended): The intermediary ~~semiconductor device~~ of claim 1, further comprising a layer of material formed overlying the walls of the second recessed region.

8. (currently amended): The intermediary ~~semiconductor device~~ of claim 1, wherein the first dielectric material is recessed below a major surface of the semiconductor substrate.

9. (currently amended): The intermediary ~~semiconductor device~~ of claim 8, wherein the first dielectric material is recessed below the major surface a distance of about 0.5 microns.

10. (currently amended): The intermediary ~~semiconductor device~~ of claim 7, wherein the layer of material comprises polycrystalline silicon.

Claims 11-25 (cancelled).

26. (currently amended): An intermediary of a semiconductor device, comprising:

a semiconductor substrate having a surface formed with a first recessed region;

a first dielectric material deposited in the first recessed region and formed with a second recessed region having a first opening and walls; and

a ~~semiconductor~~ polysilicon cap layer formed overlying the first dielectric material and having a second opening at least partially overlying ~~over~~ the first opening, wherein the ~~semiconductor~~ polysilicon cap layer and the second recessed region are configured to form a region of reduced substrate capacitance. ~~is configured to at least partially convert an oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is subsequently exposed to an oxidizing environment~~.

Claims 27-28 (cancelled).

29. (currently amended): The intermediary ~~semiconductor device~~ of claim 26, wherein the first opening is wider than the second opening.

Claims 30-31 (cancelled).

32. (currently amended): The intermediary ~~semiconductor device~~ of claim 26, wherein the second recessed region is formed having a layer of material deposited on the walls.

33. (currently amended): The intermediary ~~semiconductor device~~ of claim 32, wherein the layer of material includes polycrystalline silicon.